controlling said power control means to supply power to said memory integrated circuit at a level to maintain memory information in said memory integrated circuit during periods of no data access activity and to supply power at a level to exchange memory information with said memory integrated circuit during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

REMARKS

Claims 1-10 are pending and stand rejected. Claims 1-10 are amended. Claims 11-23 are added. Reconsideration is respectfully requested.

Objection to the Drawings and Specification

Applicant notes the Examiner's objections and will correct the discrepancies in the Formal drawings. The specification has been reviewed for grammatical errors and revised with particular attention paid to the Examiner's suggestions.

Rejections Under 35 U.S.C. §112, Second Paragraph

Claims 1-7 are rejected under 35 U.S.C. §112, second paragraph for indefiniteness. The language objected to by the Examiner has been deleted.

Rejections Under 35 U.S.C. §102

Claim 1 is rejected under 35 U.S.C. §102(b) as being clearly anticipated by Watanabe. This rejection is traversed in view of the foregoing amendment to Claim 1 and the following remarks.

Watanabe discloses in Figs. 1-2 a power supply circuit that provides one voltage output to the entire portable data

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collecting and processing apparatus. Watanabe states,

> . . . the portable data collecting and processing apparatus according to the present invention is comprised of a power supply circuit . . . whereby the apparatus is operated at a low voltage when the operation of the information processing circuit is stopped and is operated at a necessary voltage to which the voltage of a battery is boosted only when a higher voltage is needed (column 1, lines 41-54). (Emphasis added)

Thus, memory 20 must receive the same voltage as CPU 19 and input/output control circuit 12 and the rest of the apparatus.

In contrast, Claim 1, as amended, recites in pertinent part:

> power control means for supplying a variable voltage to said memory integrated circuit independently from the voltage supplied to the rest of said system;

Watanabe in no way teaches or suggests a power control means of Claim 1 because Watanabe's power supply circuit 5 supplies a single voltage to the entire apparatus and cannot supply a voltage to the memory independently. Thus, Claim 1 is not anticipated by Watanabe.

Rejections Under 35 U.S.C. §103

Claims 2, 6 and 9

Claims 2, 6 and 9 are rejected under 35 U.S.C. §103 as being unpatentable over Watanabe in view of Tuma. These rejections are respectfully traversed in view of the foregoing amendments and the following remarks.

As stated above, Watanabe fails to teach or suggest power control means as recited in Claim 1. Further, Tuma also fails to teach or suggest such power control means. Thus, Watanabe in combination with Tuma does not produce a structure according to Claim 1. Therefore, Claims 2, 6 and 9, which are dependent from Claim 1, are patentable over the cited references.

Claims 3 and 4

Claims 3 and 4 are rejected as unpatentable over Watanabe

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in view of Nanno. Applicant respectfully traverses these rejections.

Nanno no where teaches or suggests the power control means of Claim 1. Although Nanno discloses in FIG. 1 power supply control circuit 30 providing voltage VBK to blocks 17, 19 and 25, voltage VBK is merely a backup voltage of +5 VDC (column 2, lines 58-59). Thus, Watanabe and Nanno fail to teach or suggest power control means as recited in Claim 1. Consequently, combining Watanabe and Nanno does not result in a structure according to Claims 3 and 4, which are dependent from Claim 1.

Claims 5, 8 and 10

Claims 5, 8 and 10 are rejected as being unpatentable over Watanabe in view of Cole. Applicant respectfully traverses these rejections.

Cole discloses:

> The low-power memory apparatus of the present invention includes a regulated 5-volt power supply and a standby mode control device. This standby mode control device can be used to selectively supply power to the entire system, or only to the system RAM and the standby mode device, while the remainder of the system receives no power. (Column 2, lines 33-39, emphasis added).

No where does Cole teach or suggest providing "different levels of voltage" as the Examiner suggests. Instead, Cole discloses in FIG. 5 that the RAM-VCC is supplied by the voltage generated by +5V regulator Q33. Thus, it would not be possible to combine Cole and Watanabe to produce a structure according to Claims 5, 8 and 10.

Claim 7

Claim 7 is rejected as being unpatentable over Watanabe in view of Little. Applicant respectfully traverses this rejection.

Little discloses a "nonvolatile microprocessor with predetermined state on power down" (see Title). Little in no

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way teaches or suggests power control means according to Applicant's Claim 1. Claim 7 is dependent from Claim 1. Consequently, it would not be possible to combine Watanabe and Little to produce a structure according to Claim 7 because the cited reference neither teaches nor suggests power control means according to Claim 1.

New Claims 11-23

New Claims 11-20 are dependent from Claim 1 and therefore are distinguished from the cited references for at least the reasons that Claim 1 is distinguished.

Claim 21 recites in pertinent part:

> logic control means controlling said power control means to supply to said memory integrated circuit a first voltage during said first operation period, a second voltage different from said first voltage during said second operation period, and a third voltage different from said first and second voltage during said third operation period.

Claim 21 and dependent Claim 22 are distinguished from the cited references for at least the reason that none of the cited references teach or suggest logic control means according to Claim 21.

Claim 23 recites in pertinent part:

> power control means coupled to said power source for supplying a variable voltage to said memory circuit, said variable voltage being less than or equal to said substantially constant voltage provided by said power source; (emphasis added)

In contrast, Watanabe discloses:

> . . . the present invention is comprised of a power supply circuit consisting of a booster circuit for boosting the voltage of a battery . . . (Column 1, lines 43-45; emphasis added).

Thus, Watanabe teaches that output voltage is higher than the voltage supplied by the battery. Consequently, Claim 23 is distinguished from the cited references for at least the reason that none of the cited references teach or suggest power control means according to Claim 23.

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Conclusion

Claims 1-10 are pending and are rejected. Claims 1-10 are amended. Claims 11-23 are added. No new matter is added. For the reasons presented above, Applicant believes that Claims 1-23 are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested.

If the Examiner's next action is other than allowance of Claims 1-23, the Examiner is respectfully requested to call Applicants' attorney at (408) 283-1222.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on May 4, 1994

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Date of Signature

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